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㉔ Induction plasma source.

㉕ An induction plasma source for integrated circuit fabrication includes a hemispherically shaped induction coil (18) in an expanding spiral pattern about the vacuum chamber (30) containing a semiconductor wafer supported by a platen (40). The windings of the induction coil follow the contour of a hemispherically shaped quartz bell jar, which holds the

vacuum. The power source is a low frequency rf source (410) having a frequency of about 450 KHz and a power in the range of 200-2000 watts, and the pressure is a low pressure of about 0.1-100 mTorr. A high frequency rf source (420) independently adjusts the bias voltage on the wafer.

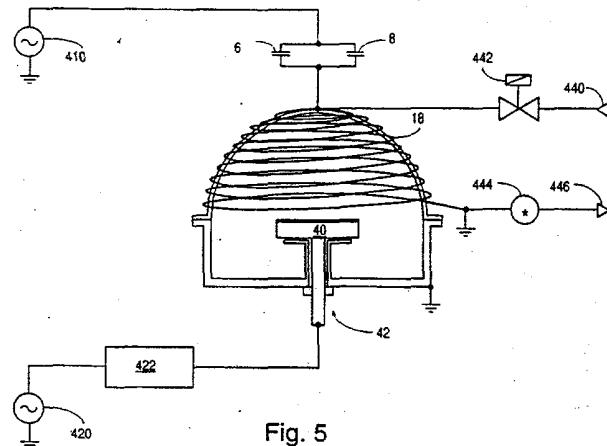


Fig. 5

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BACKGROUND OF THE INVENTIONField of the Invention

The present invention relates to plasma sources, and more particularly to induction plasma sources for integrated circuit fabrication.

Description of Related Art

Plasma etching is useful in many fields, but particularly in the field of microelectronic fabrication. Microelectronic fabrication of integrated circuits requires mass replication of tightly controlled, submicron-sized features in a variety of materials, as well as selective removal of material without causing damage to sensitive structures and remaining materials. Illustrative application of plasma etching to microelectronic fabrication of integrated circuits includes ion sputter cleaning, dielectric gap filling involving simultaneous chemical vapor deposition ("CVD") and etch, chemical blanket etchback without resist, and chemical pattern etch with resist.

Various plasma source methods and geometric designs for reactors are known for use in plasma deposition and etching. For example, electron cyclotron resonance ("ECR") sources are available from Applied Science and Technology, Inc., Woburn, Massachusetts and from the WAVEMAT Corporation, Plymouth, Massachusetts. Also, wafer cleaning and etching processes have commonly been done with equipment using various cylindrical shaped quartz vessels of various diameters having induction windings of various pitches, either constant or variable, as well as with flat spiral induction windings mounted above the dielectric chamber top plate. Radio frequency ("rf") diode and triode configurations are also known in which the wafer electrode and possibly other electrodes are powered at 13.56 MHz to produce the plasma.

Physical sputtering, one of several plasma etching mechanisms, involves the removal of material by energetic ions, which cross the sheath and transfer energy and momentum to the material being etched. As implemented on a great many of the prior art inductively coupled cavity and/or diode and triode machines, physical sputtering suffers from a number of disadvantages, including low material removal rate, poor etch uniformity due to poor ion current uniformity, and electrical damage to the substrate from ion bombardment and implantation due to high ion energies. The ECR sources provide improved performance, but with considerably greater complexity than induction-type sources.

Hence, a need continues for plasma source systems that are able to provide good ion density

to achieve high etch rates, ion current uniformity to achieve uniform removal of material over large diameter substrates, and operational stability at low pressure to achieve a more uniform ion distribution in the plasma and better directionality of ions in high aspect ratio structures, all in a generally simple machine implementation.

SUMMARY OF THE INVENTION

The present invention achieves high ion density, good ion current uniformity, and stable low pressure operation in a generally simple machine implementation.

In one embodiment of the present invention, an induction plasma source, the induction coil is hemispherical in shape. A chamber into which a substrate may be introduced is disposed inside the induction coil. In a further embodiment, the induction coil follows the contour of a hemispherically shaped vessel, which contains the chamber. In yet a further embodiment, the power source is a low frequency source having a frequency of about 450 KHz and a power in the range of 200-2000 watts, and the pressure is a low pressure of about 0.1-100 mTorr.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a cross-section view of a hemispherical induction plasma source and related components of a plasma etch system.

Figure 2 is a perspective cut-away view of the hemispherical induction plasma source of Figure 1.

Figure 3 is a plan view of the connection between the hemispherical inductor and the rf matching network of Figure 1.

Figure 4 is a plan view of the connection between the hemispherical inductor and the plasma chamber of Figure 1.

Figure 5 is an equivalent circuit of the hemispherical induction plasma source of Figure 1.

Figure 6 is a graph of etch rate versus ion source power for the hemispherical induction ion source of Figure 1.

Figure 7 is a graph of ion current uniformity for the hemispherical induction ion source of Figure 1 and a standard diode etch apparatus.

DESCRIPTION OF THE PREFERRED EMBODIMENT

A hemispherical induction plasma source 1 is shown in cross-section in Figure 1 and in a simplified perspective in Figure 2. The hemispherical induction plasma source 1 is contained within a stainless steel source housing 10 measuring 26.62 cm high and 43.82 cm wide, and includes a hemi-

spherical induction coil 18 that is provided in an expanding spiral pattern on four winding forms -- only forms 12 and 14 are illustrated for clarity. Four forms are used to simplify assembly of the induction coil 18, although other form types such as a unitary form are suitable as well, depending on the manufacturing techniques employed. The winding forms, e.g. forms 12 and 14, are made of any suitable material, which include dielectric materials such as nylon. The induction coil 18 is held in place inside channels in the winding forms, e.g. 12 and 14, by any suitable dielectric strapping, adhesive, or cement. The winding forms, including forms 12 and 14, are securely attached to the housing 10 in any convenient manner, as by bolts or adhesive.

The induction coil 18 is copper tubing having an inner diameter of 3.0 mm and an outer diameter of 4.75 mm. The hemispherical induction coil 18 has a radius to centerline of 7.75 cm. The expanding spiral pattern of the induction coil 18 is made of thirty-six windings. The first winding is nearly coplanar with substrate 32 and each subsequent winding spirals upward with a 2.432 degree angular displacement for a total of 36 coils.

During processing operations, the induction coil 18 is positioned about a vacuum chamber 30 contained within a quartz vessel or bell jar 20, in conjunction with a stainless steel chamber top plate 24 of any suitable thickness, illustratively 1.91 cm thick. Preferably, the vessel 20 is hemispherically shaped so that there is a balanced coupling of rf (uniform dielectric spacing) into the vacuum cavity. Generally, the vessel material is an insulating dielectric having sufficient structural integrity to withstand a vacuum. Suitable materials include quartz, pyrex, aluminum oxide (Al_2O_3 , also known as sapphire), polyamide, and other oxide or nitride composites. Illustratively, the radius of the vessel 20 is 17.78 cm, and the vessel material is quartz having a thickness of 0.51 cm. The induction coil 18 follows the hemispherical contour of the vessel 20, which is capable of holding a vacuum and contains the substrate, illustratively a semiconductor wafer 32 containing integrated circuit chips in fabrication.

The housing 10 is mounted onto the chamber top plate 24 in any convenient manner. Figure 1 shows the housing 10 as being engaged by an rf seal 22, which includes copper leaves to prevent spurious rf emissions from the induction plasma source 1.

The semiconductor wafer 32, illustratively 200 mm in diameter, is supported within the chamber 30 by an electrically conductive (e.g. stainless steel) wafer support pedestal 42 that includes a platen 40 having a stainless steel portion 44 underlying the wafer 32 and a ceramic dark space ring 46 extending beyond and in the plane of the platen

portion 44. The diameter of the portion 44 is 18.35 cm, and the outer diameter of the dark space ring 46 is 28.62 cm. Under the platen 40 is a dark space shield 50, which has an outer diameter of 20.32 cm.

The pedestal 42 is capable of vertical motion, which is imparted by any suitable mechanism (not shown). The position of the pedestal depends on whether the plasma etch system is operating in process mode or in wafer transfer mode. In process mode, the platen 40 is positioned within the chamber 30, as shown in Figure 1. Bellows 52, which is provided to isolate the mechanical components of the pedestal drive system at atmospheric pressure from the vacuum in chambers 30 and 60, is well extended. The wafer 32 rests on the pedestal 40, within the process chamber 30.

For wafer unloading and loading, the pedestal 40 is lowered into a wafer transfer region 60, which is 7.54 cm in height and includes at one end a sealable wafer transfer opening 26 having a height of 4.60 cm. The bellows 52 is well compressed, and three lifter pins --only pins 54 and 56 are shown -- protrude through holes (not shown) in the platen 40 so as to support the wafer 32 in a stationary position within the transfer region 60 as the pedestal 42 lowers. The sealable wafer transfer opening 26 is provided to permit a wafer transport arm (not shown) access beyond the wafer transfer flange 28 into the transfer region 60 during wafer transfer mode. Suitable wafer transport arms and associated mechanisms are well known in the art. In a wafer transfer operation, tines on the end of the transport arm are inserted under the wafer 32 as it is supported by the lifter pins (e.g. pins 54 and 56). The transport arm is raised to lift the wafer 32 off of the lifter pins, so that when the transport arm is retracted, the wafer 32 is removed from the transfer region 60. A new wafer is substituted on the tines, and the transport arm is then moved into a position over the lifter pins (e.g. 54 and 56). The transport arm is lowered to deposit the wafer 32 onto the lifter pins, and then withdrawn. The pedestal 42 is raised to cause the wafer 32 to be deposited on the platen 40.

The induction source 1 is suitable for use in a variety of applications, including ion sputter clean, chemical blanket etchback, chemical pattern etch, and plasma-enhanced chemical vapor deposition ("PECVD"). Ion sputter clean involves the use of a plasma obtained from a suitable inert gas such as argon at low pressure to remove material from the surface of the substrate by momentum transfer. In the illustrative arrangement of the induction system 1 for etch clean shown in Figure 1, argon gas is introduced into the chamber 30 through a single port 58 (Figure 1) located in the chamber sidewall just below the platen 40. Chemical etching uses

reactive gases instead of an inert gas in typically a higher pressure regime than an ion sputter clean, and is suitable for etchback or for pattern etch where a photoresist or other masking material is present. Because of the higher pressure or greater reactivity of species, an arrangement of the induction system for chemical etching (not shown) preferably uses a symmetrical multiple port arrangement about the substrate for introducing the reactive gases. PECVD uses different reactive gases that induce film deposition. An arrangement of the induction system for PECVD (not shown) preferably uses the symmetrical multiple port arrangement. When used with careful substrate bias control, the induction system for PECVD is suitable for dielectric gap filling.

A vacuum system (not shown) of any suitable type is connected to the transfer region 60 for evacuating the chamber 30. Suitable vacuum systems are well known in the art. After chamber 30 is evacuated, process gas, which for an ion sputter clean is preferably argon, is furnished to the chamber 30 through the port 58 to attain a desired pressure of process gas. Illustratively for an ion sputter clean, sufficient argon is introduced to establish a low pressure in the range of about 0.1-100 mTorr, and preferably 0.1-10 mTorr.

The radio frequency ("rf") subsystem of the induction plasma source 1 includes matching capacitors 6 and 8, which are enclosed within a stainless steel rf match enclosure 2. Capacitors 6 and 8 are connected to bus bars (only bus bar 4 shown), and the assembly is mounted onto a dielectric block 5 which is mounted on the housing 10.

The induction coil 18 is coupled to the rf matching network capacitors 6 and 8 as shown in the detail of Figure 3. Capacitors 6 and 8 each have one terminal screwed into the copper bus bar 4 and the other terminal screwed into copper bus bar 204. Bus bar 4 is connected to the low frequency source 410 (Figure 5). Bus bar 204 is connected to end 206 of the copper tubing of which the induction coil 18 is formed through fitting 208. Fitting 208 is screwed into a channel through the bus bar 204. Another fitting 210 is screwed into the other end of the channel. Teflon tubing 212 is connected to the fitting 210 for delivering a cooling fluid. The induction coil 18 is coupled to the grounded top plate 24 as shown in the detail of Figure 4. Bus bar 302 is bolted to the housing 10 by bolt 304, and is connected to end 306 of the copper tubing of which the induction coil 18 is formed through fitting 308. Fitting 308 is screwed into a channel through the bus bar 302. Another fitting 310 is screwed into the other end of the channel. Teflon tubing 312 is connected to the fitting 310 for draining a cooling fluid.

The rf subsystem of the induction plasma source 1 is represented in Figure 5. The power source includes a low frequency source 410 and a high frequency source 420. The low frequency source 410 has a frequency of about 450 KHz and a power in the operating range of 200-2000 watts. The low frequency source 410 is connected to the induction wiring 18 through a low frequency matching network that includes the capacitors 6 and 8, connected in parallel. The low frequency matching network is tuned to couple low frequency rf energy into the plasma cavity in accordance with the cavity shape, pressure, and plasma chemistry, in a manner well known in the art. Illustratively in this embodiment, capacitors 6 and 8 are transmitting-type mica capacitors, each having a value of 1200 pF at 6000 rated volts. The high frequency source 420 has a frequency of about 13.56 MHz and a power in the operating range of 25-500 watts. The high frequency source 410 is connected to the platen 40 through an autotune high frequency matching network 422 such as, for example, model AM-5, available from RF Plasma Products, Inc. of Kresson, New Jersey. The autotune matching network 422 has an internal dc bias control that allows a regulated bias voltage at the wafer 32 to be achieved.

The induction coil 18 is cooled by any suitable liquid, an example of which is chilled water. Chilled water is introduced to the induction coil 18 from source 440 through valve 442, and is returned to sink 446 through flow switch 444. Illustratively, the chilled water is delivered at a pressure in the range of 3-5 bars, for example.

Although the induction plasma source 1 is mechanically uncomplicated and relatively simple to manufacture, it advantageously achieves high ion density, good ion current uniformity, and stable low pressure operation. When used for argon ion sputter cleaning, the uniform high density ion flux generated by induction plasma source 1 provides, in combination with a suitable high frequency bias applied to the wafer 32, a gentle, low voltage argon sputter particularly suitable for the removal of thin oxides and contaminants prior to the deposition of thin metal films. This gentle, low voltage argon ion sputter clean avoids gate damage that could occur during contact cleaning at higher energies. The argon ion sputter clean is also advantageously used to remove thin native oxides in contacts and vias, including those down to the silicon substrate, which provides for decreased contact resistance to the first level layer due to the removal of native oxide as well as the reduction in the amorphization of the silicon surface.

Illustrative characterization data is presented in Figures 6 and 7. Figure 6 is a graph of etch rate as expressed in angstroms/minute versus ion source power as expressed in watts for various wafer bias

voltages ($V_{dc} = -50V, -75V, -100V$), the hemispherical induction plasma source 1 operating on thermal oxide wafers at a pressure of 0.6 mTorr of argon. The actual sheath potential (total voltage seen at the wafer surface) is approximately 30 volts greater than the wafer bias voltage. Figure 6 shows that high etch rates are achieved at very low voltage levels. At 200 watts ion source power (source 410), an etch rate of about 250 Å/min is achieved for a wafer bias voltage of -100 volts, decreasing only to about 200 Å/min (about 20% decrease) at a wafer bias voltage of -50 volts (50% decrease). At 400 watts ion source power, an etch rate of about 600 Å/min is achieved for a wafer bias voltage of -100 volts, decreasing only to about 450 Å/min (about 25% decrease) at a wafer bias voltage of -50 volts (50% decrease). At 600 watts ion source power, an etch rate of about 950 Å/min is achieved for a wafer bias voltage of -100 volts, decreasing only to about 700 Å/min (about 26% decrease) at a wafer bias voltage of -50 volts (50% decrease). At 800 watts ion source power, an etch rate of about 1200 Å/min is achieved for a wafer bias voltage of -100 volts, decreasing only to about 900 Å/min (about 25% decrease) at a wafer bias voltage of -50 volts (50% decrease).

Figure 7 is a graph expressing ion current uniformity as a function of ion current in milliamperes versus radial position in centimeters. Curve 602 represents the ion current across a wafer in a sputter clean process using the hemispherical induction ion source of Figure 1 at a pressure of 0.6 mTorr of argon and a wafer bias voltage of minus 100 volts. Ion current varies only about $\pm 1.1\%$. Not only is the ion current above the pedestal 40 uniform, but the ion current is quite high at about 6 mA, even despite the low pressure operation at 0.6 mTorr. Curve 604 represents the ion current across a wafer in a sputter clean process using a conventional diode etch at a pressure of 20 mTorr and a wafer bias voltage of minus 700 volts. Ion current varies about $\pm 12.9\%$.

Hence, when used with dual power supplies to independently control the ion-current and the ion energy at the wafer surface, the hemispherical induction plasma source 1 allows high etch rates to be achieved while minimizing the total voltage seen at the wafer 32. High ion densities of greater than 1×10^{11} (ions/cm³) yield excellent etch rates of greater than or equal to 300 angstroms/minute for thermal oxides at total wafer voltages of less than 150 volts.

To understand the reasons for the significantly improved results achieved by the relatively simple hemispherical induction plasma source 1, consider first the general principle that both gas pressure and frequency have an effect on sheath potentials. As pressure is lowered below about 50 or 100

mTorr, the sheath thickness and voltage across the sheath begin to increase in many plasma systems from tens of volts to hundreds of volts or more, as typified by the diode etch characterization shown in curve 604 of Figure 7. Correspondingly, the plasma potential goes up and the ion-substrate bombardment energy rises sharply with decreasing pressure. These effects are a consequence of longer mean free paths and reduced collision rates between electrons and molecules. Electron energy and potentials increase in order to raise the probability of ionization and sustain the plasmas, despite the lower collision rates. Lower rf excitation frequency has a similar influence on diode systems. When gas pressure is in the range of about 100 to 1000 mTorr and frequency is lowered from about 10 MHz to less than about 1 MHz, once again sheath potentials increase dramatically and favor energy-driven ion assisted etching. The potential increase is attributed to a change in the plasma sustaining mechanism.

Hence, in general terms for diode systems, frequency and pressure are interchangeable variables, and either low frequency or low pressure increases sheath potentials, which helps sustain the plasma, but which also tends to damage the substrate and cause gate damage in MOSFET devices. For this reason, a more efficient method of ionization should be employed.

The hemispherical induction source 1 achieves a gentle, low voltage, high rate argon ion sputter clean at low pressure that avoids gate damage that could occur during contact cleaning at the higher energies typically observed with other plasma sources. We believe that the advantageous performance characteristics of the hemispherical induction plasma source 1 can be explained as follows. Induction discharges are sustained in the induction plasma source 1 during low pressure operation (e.g. 0.6 mTorr and below) by the induced azimuthal electric field near the wall of the vessel 20. The oscillating current in the excitation coil produces an axial, time-varying magnetic field which induces an oscillating azimuthal electric field. Electrons entering the region within the plasma boundary near the induction coil 18 are accelerated azimuthally and produce an electric current opposite to that in the induction coil 18. This results in the axial magnetic field being mostly cancelled in the interior of the plasma discharge. Consequently, the magnitude of the electric field is very low in the interior of the chamber 30.

The exterior part of the plasma near the induction coil 18 is the main region in which energy is transferred to the plasma electrons. These electrons rapidly diffuse through the plasma volume due to the elastic scattering collisions with the atoms of the gas. The electrons, which have en-

ergy of about 20 eV, make ionizing collisions with atoms throughout the chamber 30. In the induction plasma source 1, at gas pressures well below a milliTorr (e.g. 0.6 mTorr) the likelihood is that about 1 collision per ion occurs from creation of the ion to when it hits the wall after a mean free path of average length of about 10 cm, which is essentially a free fall to the wall. Contrast the low pressure case from the case at higher pressures of several milliTorr, when more than 10 collisions occur over such a path length. In this case, the ions diffuse to the wall.

The spatial dependence of the ionization rate is highly dependent on the pressure and electron mean free path for scattering, since the electrons are energized at the outer wall near the induction coil 18. When the pressure is very low (0.6 mTorr), the mean free path for the electrons is such that they normally transit the vessel without a collision. However, the path length of the electron in the inductive field is increased more than 100 times that of an electron moving in the electric field of a diode (parallel plate) system of comparable size. The inductive source also allows ionization events to occur in a very large volume (at the perimeter) which contrasts to the diode ionization mechanism which occurs mostly at the sheath boundary through "wave riding" and secondary injection. One might explain the very uniform ion current above the electrode as follows. The likelihood of an electron making ionizing collisions is smaller in the center than nearer the walls since they need not pass through the center. Nonetheless, since the height of the plasma column above the center is greatest, the current falling on the center of the electrode is nearly equal to that falling on the edge where the plasma column is not so tall but where the ionization rate is larger.

The sputter rate is dependent on the high frequency bias voltage. The observed sputter rates for, e.g., SiO_2 correlates well with the ion current density because the sheath potential is quite constant over the surface of the wafer 32 and the sputter rate is simply the product of the ion current density and the sputter efficiency, which is a function of the ion energy. The sheath potential is shown to be uniform because the time averaged potential in the plasma just above the electrode surface of the pedestal 40 (at about 1.9 cm) is constant over the area of the pedestal electrode, while the potential on the pedestal electrode surface itself is independent of position. The sheath potential, therefore, which is the difference of the plasma and electrode surface potentials, is also essentially uniform.

While the invention has been described with respect to the embodiments set forth above, the invention is not necessarily limited to these em-

bodiments. Accordingly, other embodiments, variations and improvements not described herein are not necessarily excluded from the scope of the invention, which is defined by the following claims.

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means for inducing a low frequency oscillating azimuthal electric field in a region near the quartz wall so that electrons entering the region within the plasma boundary are accelerated and cancel an axial magnetic field in the interior of the plasma discharge; and

means for imposing a biasing voltage on the wafer independently of the inducing means.

9. A plasma process apparatus for integrated circuit wafer fabrication, comprising:

a housing having a top plate;

a bell jar having a hemispherical quartz wall, the bell jar being mounted on the top plate for containing a vacuum chamber;

a platen having a top surface for supporting a semiconductor wafer in the vacuum chamber;

a hemispherical induction coil conformal with the quartz wall of the bell jar, the induction coil having a plurality of windings which are generally parallel to the platen, one of the windings being at the base of the induction coil and generally coplanar with the top surface of the platen;

a gas system for delivering gas to the process chamber;

a low frequency radio frequency power source connected to one end of the induction coil through a matching network for inducing an oscillatory azimuthal electric field within the process chamber near the bell jar wall, the other end of the induction coil being connected to the housing; and

a high frequency radio frequency power source connected to the platen through a matching network for biasing the wafer;

wherein a plasma is operably sustainable in the vacuum chamber at a gas pressure therein as low as 1.0 milliTorr.

10. An apparatus as in claim 9 wherein the windings of the induction coil form a single layer hemispherically shaped expanding spiral having an internal volume sufficiently large to contain the bell jar.

11. An apparatus as in claim 9 wherein the windings of the induction coil are a copper tube, further comprising a cooling system for circulating a cooling fluid through the copper tube to cool the induction coil.

12. An apparatus as in claim 9 wherein a plasma is operably sustainable in the vacuum chamber at a gas pressure therein as low as 0.6 milliTorr.

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13. An apparatus as in claim 9 wherein a plasma is operably sustainable in the vacuum chamber at a gas pressure therein as low as 0.1 milliTorr.

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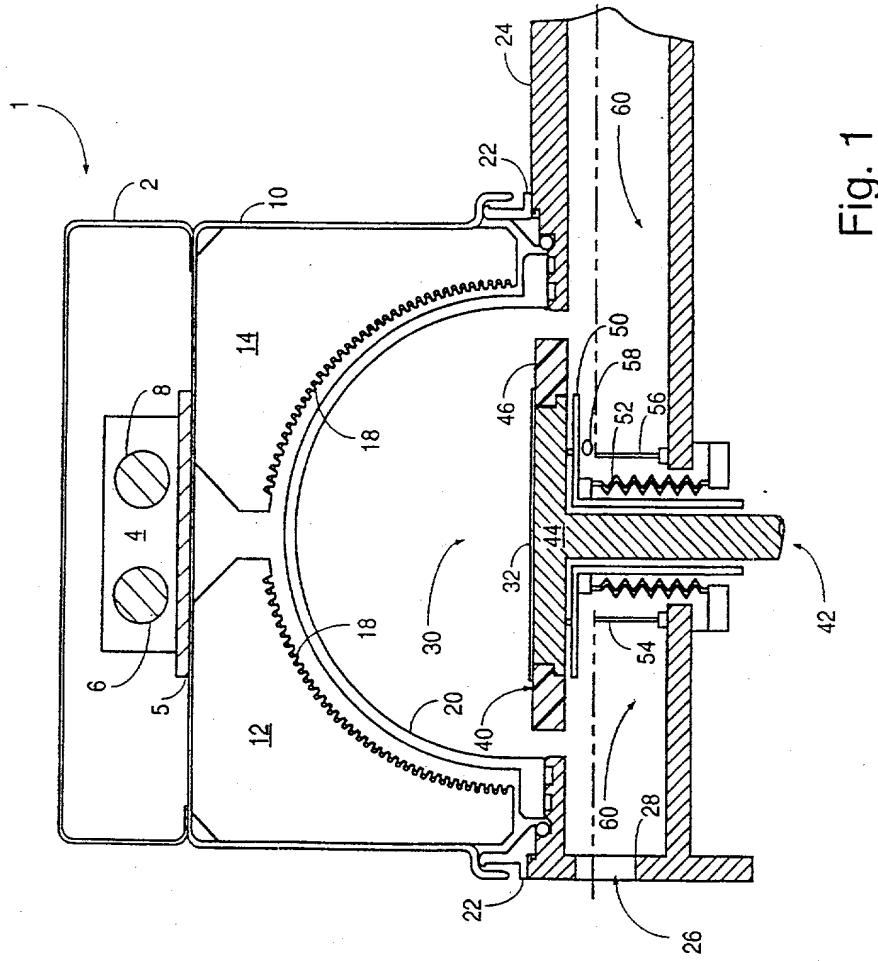


Fig. 1

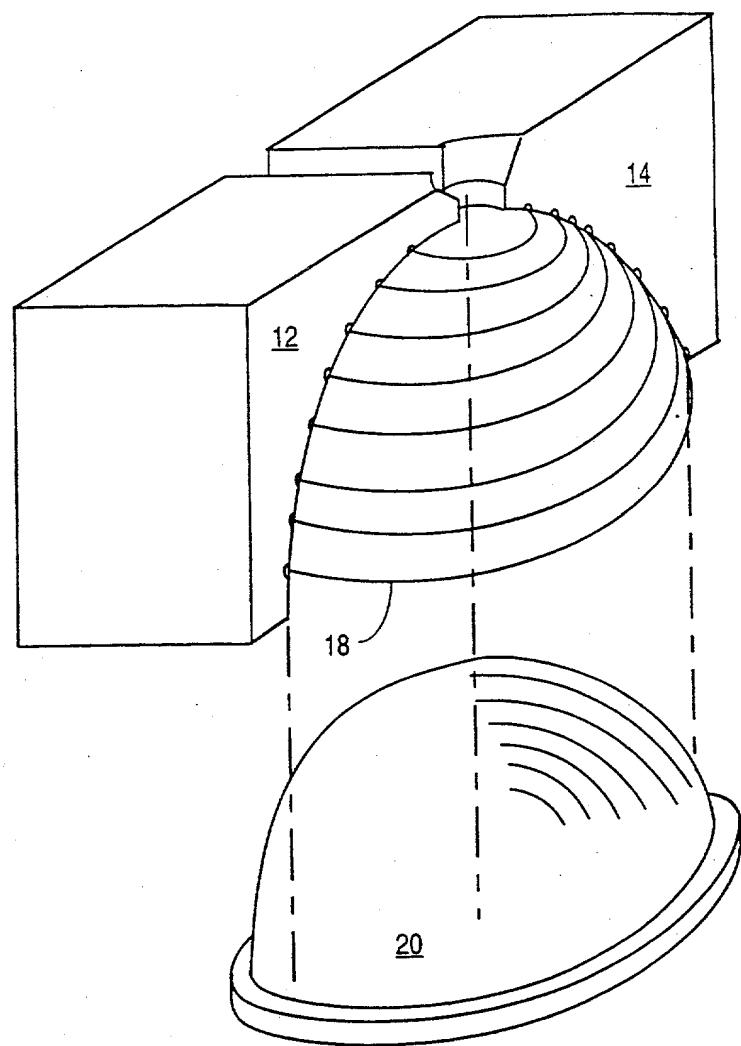


Fig. 2

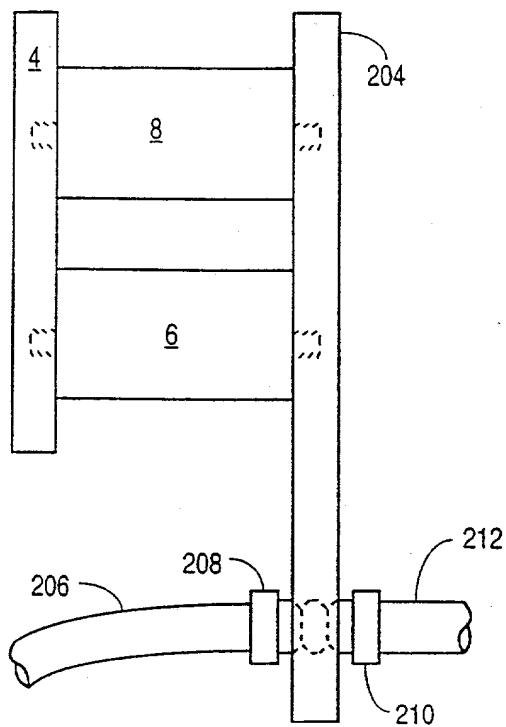


Fig. 3

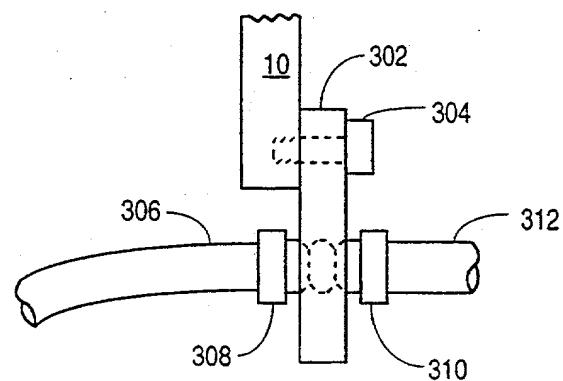


Fig. 4

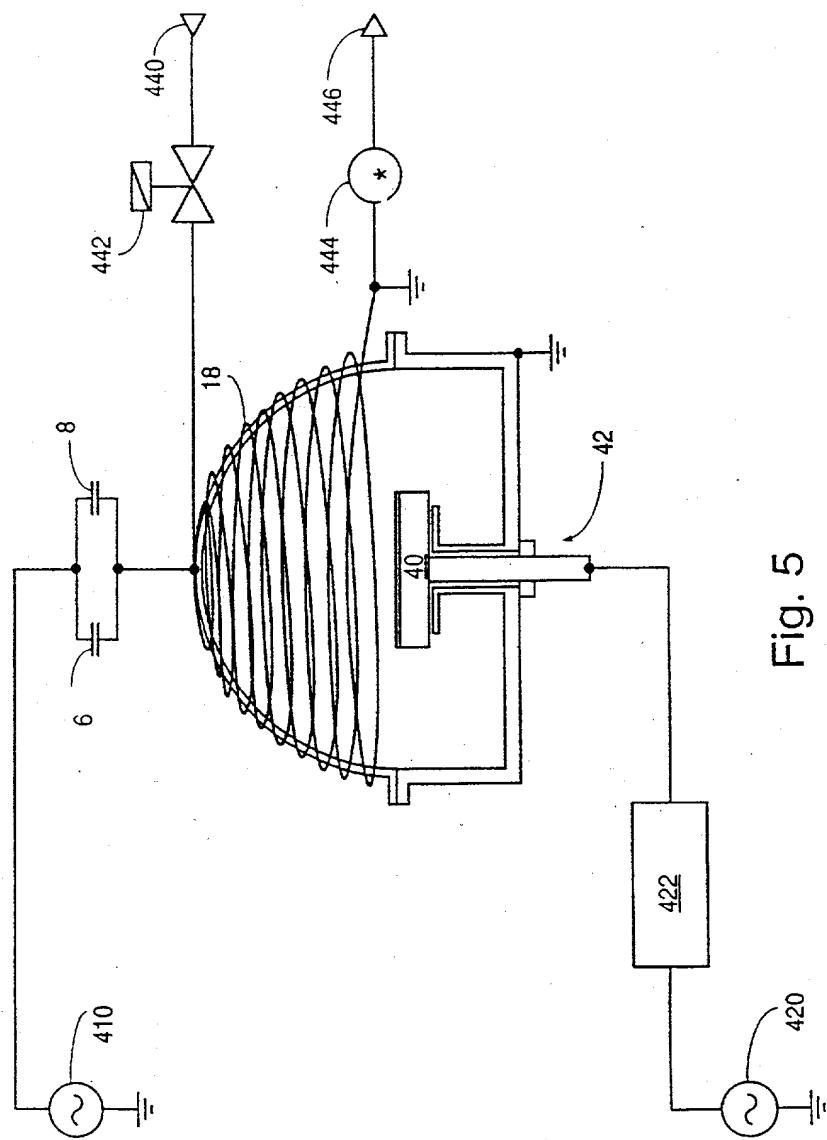


Fig. 5

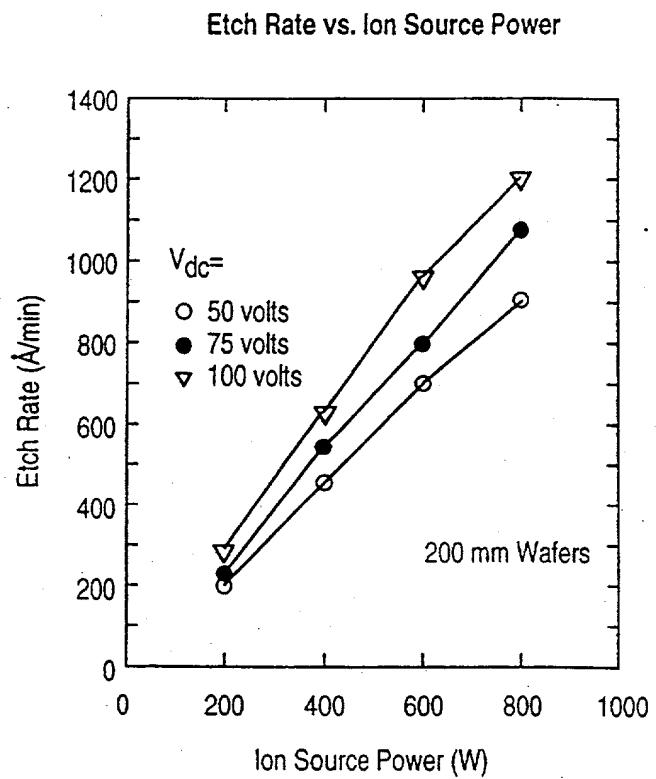


Fig. 6

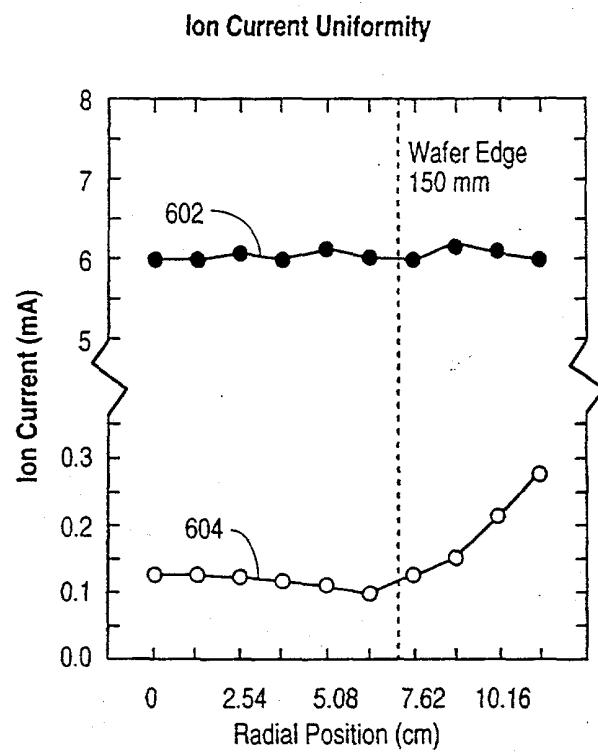


Fig. 7



DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.S)
A	US-A-4 948 458 (OGLE) * column 3, paragraph 1 -paragraph 2 * * column 5, line 33 - column 6, line 16 * * column 6, line 60 - column 7, line 10; figures 1-4,6 *	1,3,4, 6-10,12, 13	H01J37/32 H05H1/46
A	GB-A-2 231 197 (NORDIKO LTD) * page 1, paragraph 1 * * page 7, line 4 - line 33 * * page 12, line 27 - page 13, paragraph 1; figures 1,2 *	1,2,8,9	
A	US-A-4 431 901 (HULL) * column 1, paragraph 2 * * column 1, line 51 - line 68; figures 1,2 *	5,11	
A	EP-A-0 489 407 (APPLIED MATERIALS) * abstract * * page 5, line 48 - line 58; figure 1 *	3,4	TECHNICAL FIELDS SEARCHED (Int.Cl.S) H01J H05H
The present search report has been drawn up for all claims			
Place of search THE HAGUE	Date of completion of the search 24 January 1994	Examiner Greiser, N	
CATEGORY OF CITED DOCUMENTS		T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document	
X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document			